WHEN IS A NAND STACK NOT A STACK???

With some recent technology advances in NAND memory, I am seeing a lot of confusion on the use of the term "stack". I will attempt to give a simplified view on different definitions.

If you are a wafer processing expert, you can ignore this overview blog and we can argue details and pros/cons by Zoom.

OVERVIEW OF STACKS AND NON-STACKS

- **Die stacks**: This is where we stack one NAND die (a silicon chip) on top of another, wire bond it out and put it all in one package. we have been doing this on memory for well over 20 years. 16 die stacks are available from everyone so if our base die is 512 Gbits, we can get a 8Tbit (1Tbyte) package.
  - Pros: more memory in a package
  - Cons: cost is cost of 2 die plus packaging and test cost (its not a cost reduction)

- **3D NAND** layers: These are not stacks but some people still use the term. NAND Layers are "stacked up" on wafer in a series of depositions and then a channel hole is made through the "stack". we are shipping ~96 Layer NAND today
  - Pros: as you go from 64 to 96 Layers you get ~50% more bits for an additional process 10% cost adder (oversimplified). so its a big bit cost reduction
  - Cons: etching that hole and filling it and making it all work is not that easy (see next)

- **String Stacking**: If you want to go from 64 to say 128 Layers but you cannot etch and fill the hole, you can do it in two steps. Do 64L, dep and etch hole and fill. Then do another 64L dep etch and fill hole. This is string stacking and everyone but Samsung has been forced to do this so far. Samsung will do it in the future.
  - Pros: you get your layers increased and lower cost
  - Cons: two step approach is more expensive than single stack (say 5%)

- **Wafer bonding**: Instead of doing die stacks, you can bond (call for details) two wafers face to face, then dice them. This is used for wafer that are not the same technology process. YMTC is now doing this on their Xstacking process for 64L.
    - Pros: you get logic and array "stacked" on top of one another for small die size and each wafer optimized
    - It is expensive, complex, and requires additional post stack processing

There are processes with interposers like HBM used for DRAM, TSVs, stacking DRAM on NAND and a processor.... etc but I will save those for a different blog.

I prefer the terms I use, but it is important to not get these confused as the benefits and cost are completely different

I can go through details on cost for each and how they are done and complexities. These provide much of the competitive strengths of each company. Call/email for more info

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